Conventionally, a nonvolatile semiconductor memory of this kind is manufactured according to a process order shown in Figs. 10A to 10C and 11A to 11C. Figs. 10A to 10C are cross sections in an X-X direction in Fig. 1A. Figs. 11A to 11C are cross sections in a Y-Y direction in Fig. 1A. Here, Fig. 1A is a plan view of a nonvolatile semiconductor memory according to an embodiment of the present invention, but Fig. 1A is also used to explain a conventional technique.

A1

*Replace the paragraph beginning at page 2, line 15, with the following rewritten paragraph/s:*

Subsequently, photolithography is performed to form a photoresist (not shown) in stripes extending in the Y-Y direction. Arsenic (As) ion implantation is performed by using this photoresist and the first conductive layer 3 patterned in stripes as masks under conditions of an acceleration energy 15 keV and a dose of $4.5 \times 10^{15}$ ions/cm$^2$ so as to form an n-type high-concentration impurity diffusion layer 5 in the low-concentration impurity diffusion layer 4. These impurity diffusion layers 4, 5 are used as a source/drain region i.e. a bit line.

A2

*Replace the paragraph beginning at page 18, line 7, with the following rewritten paragraph/s:*

Subsequently, as shown in Fig. 5D, thermal oxidation is performed in an oxygen atmosphere at e.g. 850°C for 20 minutes so as to oxidize the sidewalls of the floating gate 3 and the control gate 8 composed of polysilicon via the second insulating film 10.

A3

Consequently, a silicon oxide film 11 composed of polysilicon having a thickness of 20 to 30 nm is formed on sidewalls of the floating gate 3 and the control gate 8. In this case, as shown in Fig. 6 which is an enlarged view of a portion P2 enclosed with a broken line in Fig. 5C, oxidation of the grain boundary 13 between polysilicon grains 12 constituting the floating gate 3 is suppressed and uniform oxidation occurs at the interface between the floating gate 3 and its surrounding insulating films 10 and 11.

A3 cont'd

**IN THE CLAIMS**

Please substitute the following amended claim(s) for corresponding claim(s) previously presented. A copy of the amended claim(s) showing current revisions is attached.

1. (Amended) A method for manufacturing a nonvolatile semiconductor memory including memory cells formed in a matrix on a semiconductor substrate, wherein each memory cell comprises a tunnel oxide film, a floating gate, a first insulating film and a control gate stacked in this order, the method comprising:

A4

forming the tunnel oxide film on the semiconductor substrate;

forming a first conductive layer to be used as a material of the floating gate on the tunnel oxide film;

patterning the first conductive layer in stripes extending in one direction;